

FIG. 1 is a block diagram of a memory array 100. The array 100 includes a first memory array 110 and a second memory array 112. The first memory array 110 includes a first set of memory cells 130 and a first memory cell 160. The second memory array 112 includes a second set of memory cells 132 and a second memory cell 162. The array 100 also includes an address decoder 120. The address decoder 120 is connected to the first memory array 110 and the second memory array 112. The array 100 further includes a first sense amplifier 140 and a first latch 142. The first sense amplifier 140 is connected to the first memory array 110 and the first latch 142. The array 100 also includes a first sense amplifier 180 and a first latch 182. The first sense amplifier 180 is connected to the first memory array 110 and the first latch 182. The array 100 also includes a second sense amplifier 180 and a second latch 182. The second sense amplifier 180 is connected to the second memory array 112 and the second latch 182.

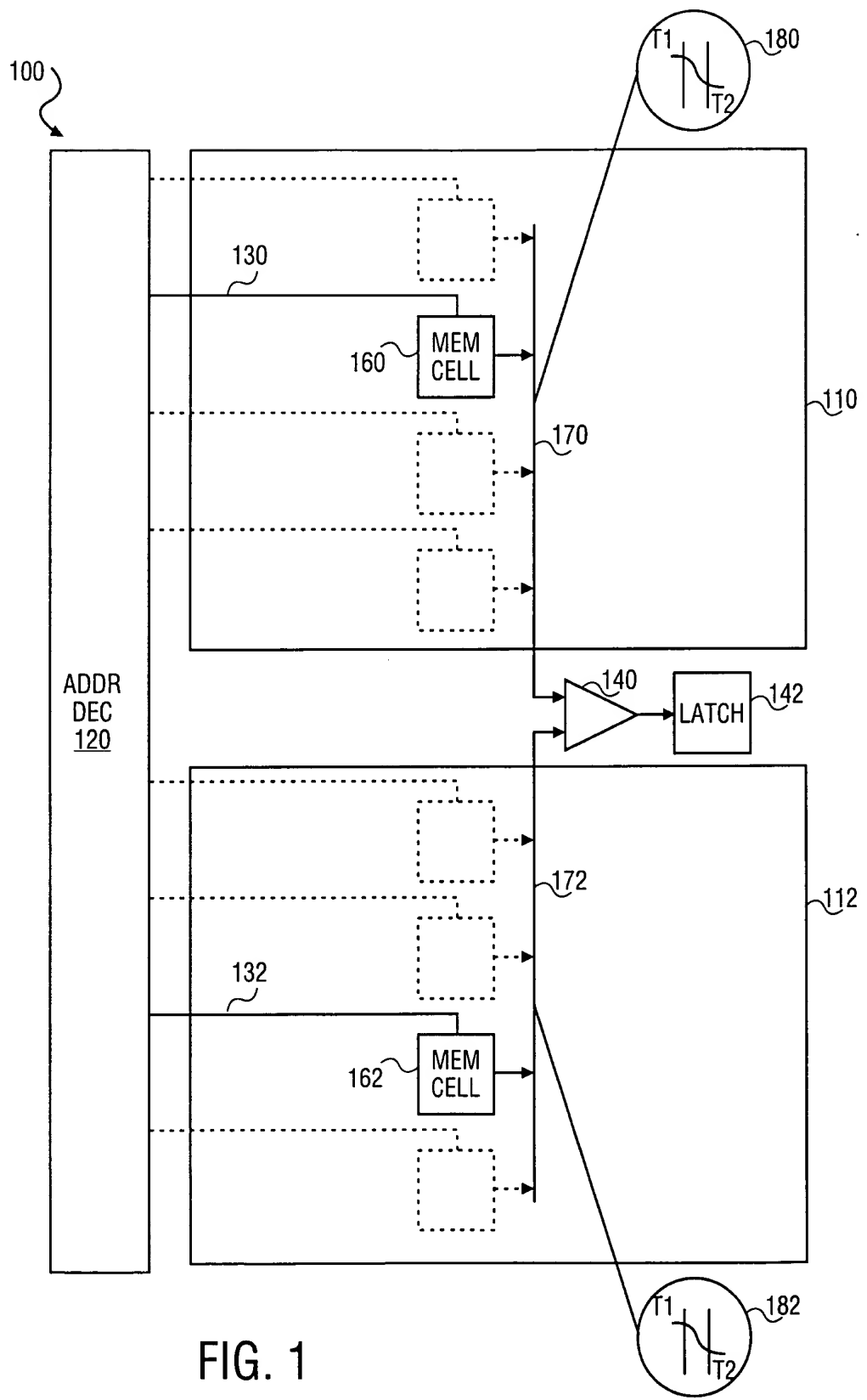


FIG. 1



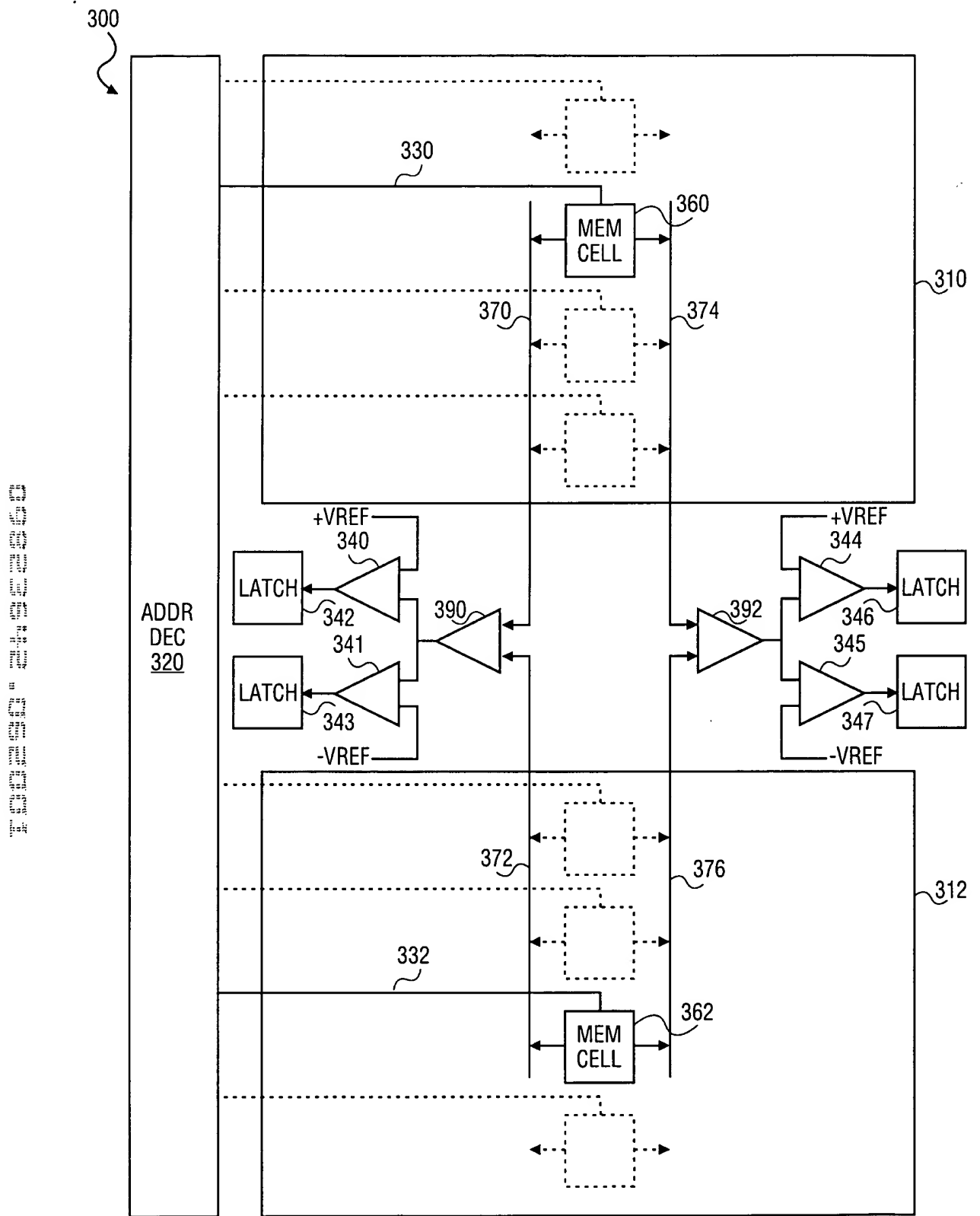


FIG. 3

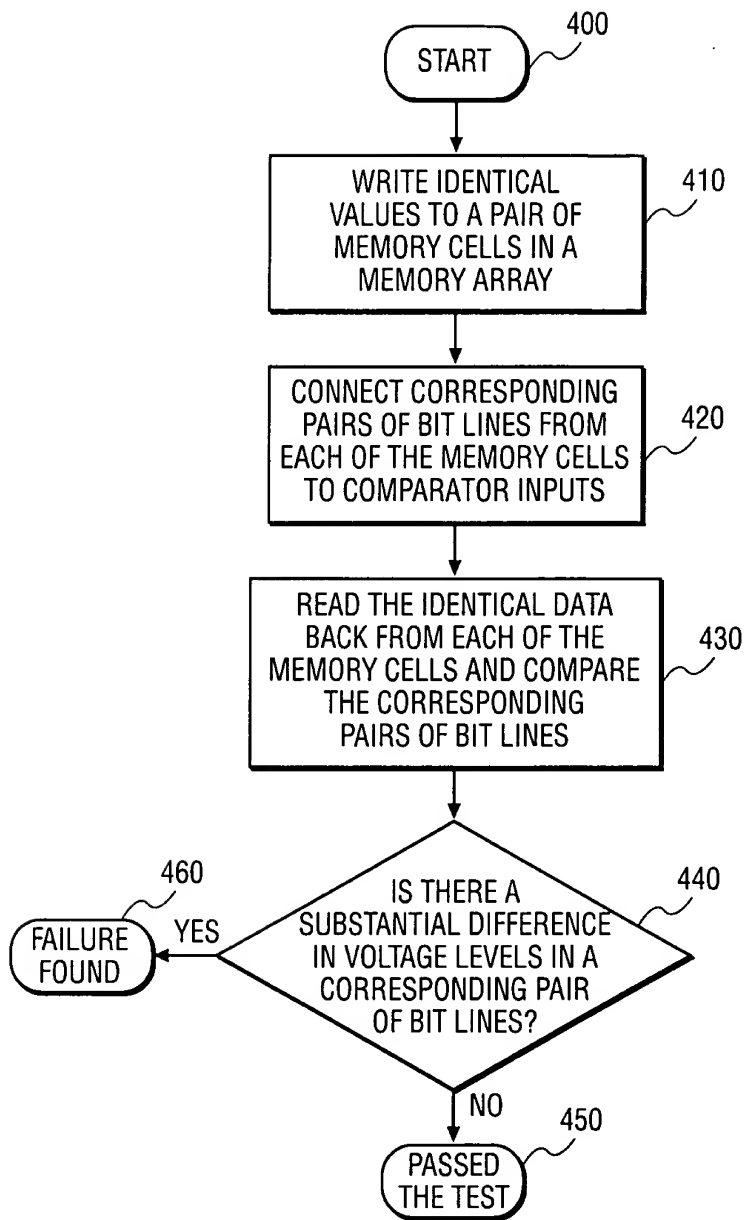


FIG. 4

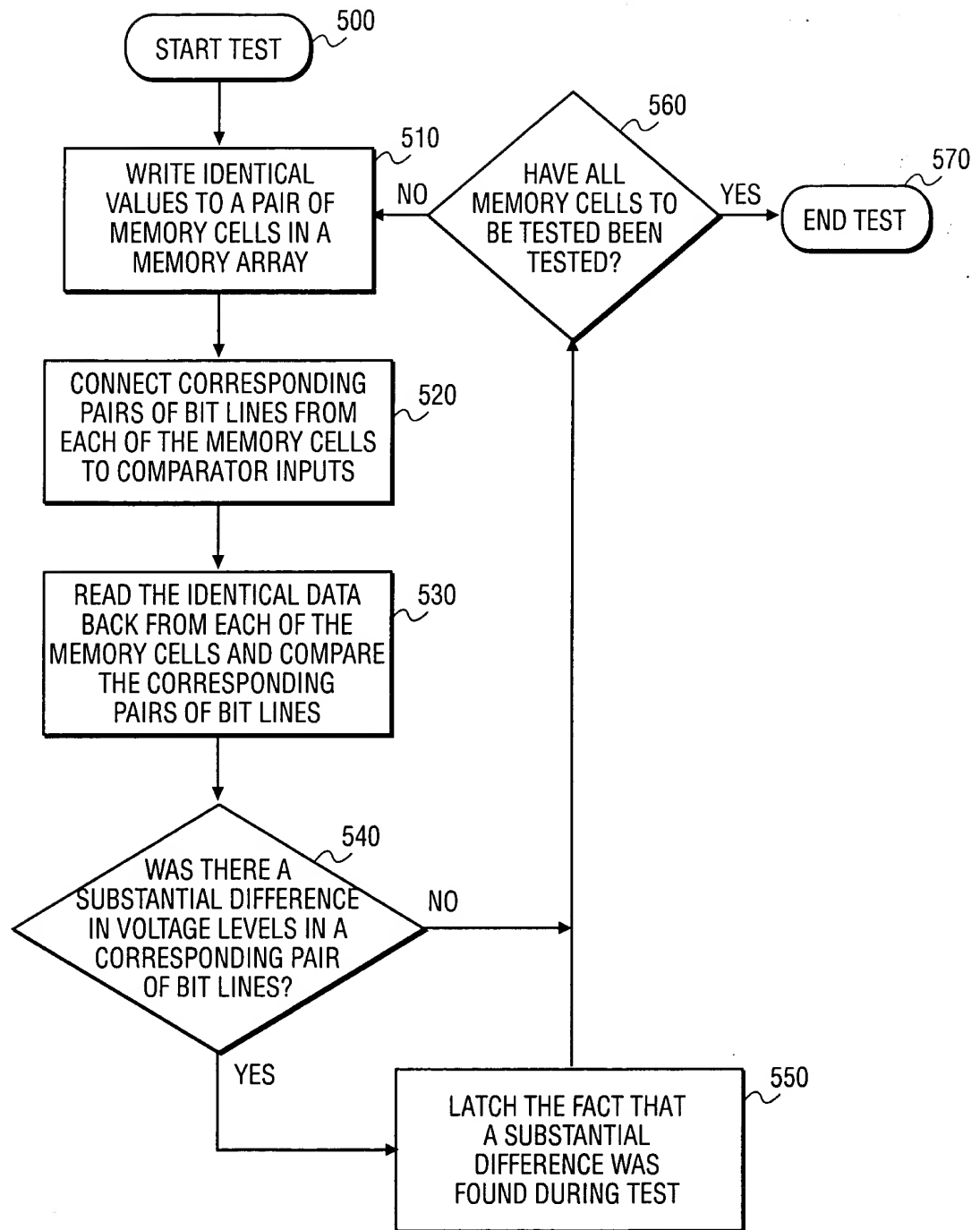


FIG. 5

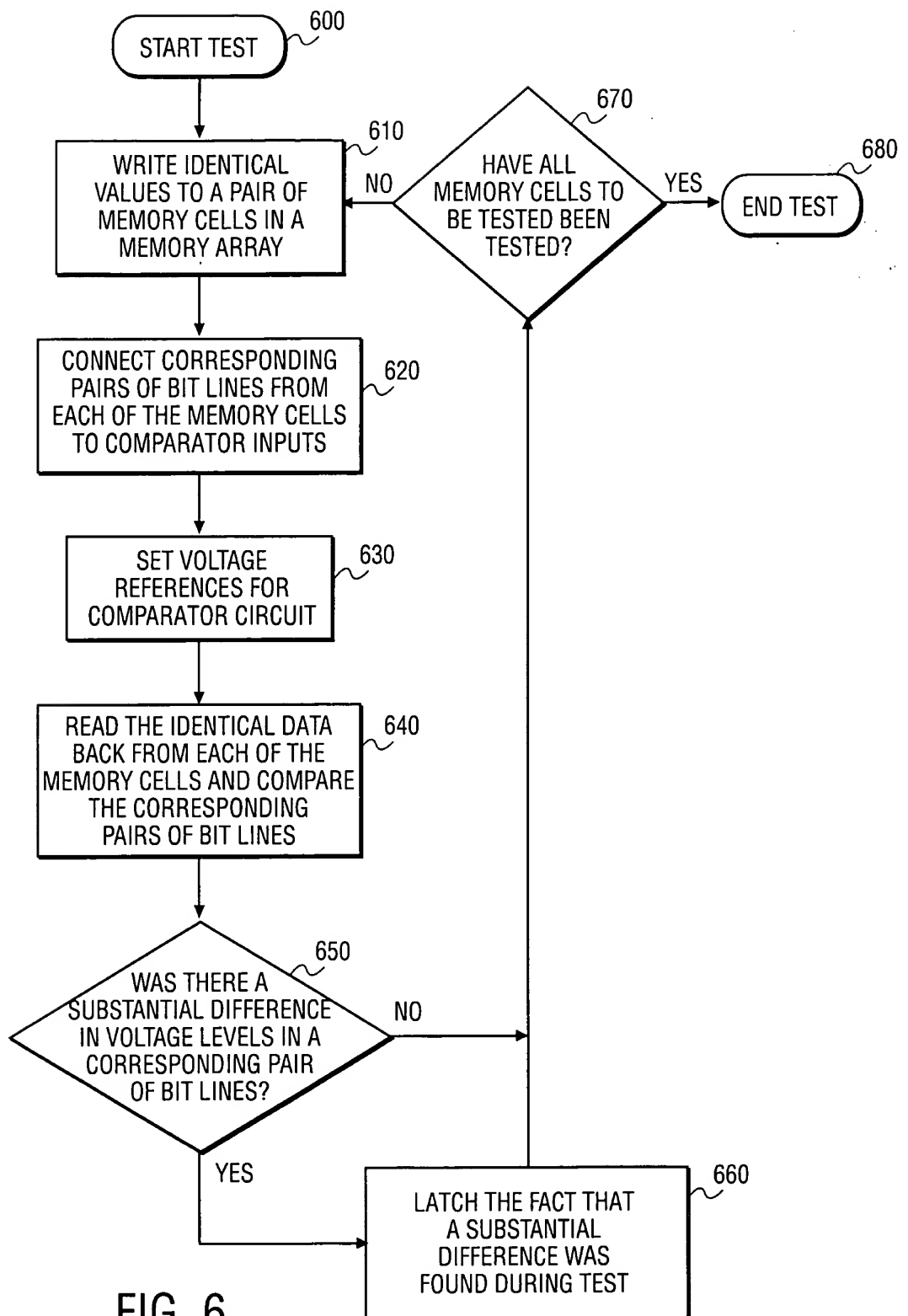


FIG. 6